



Data Sheet

NT99142

1/4" HD CMOS Image Sensor

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1. Features

- Low dark current
- Auto black level calibration
- Two wire serial interface, 16-bit address and 8-bit data
- Support output format: YCbCr (4:2:2), Raw
- Support image size: HD (1280 x 720), and any size from scaling down
- Lens shading correction
- Automatic control functions:
 - Auto-Exposure control (AE), Auto-White Balance (AWB)
- Including: Sharpness, noise reduction, defect correction, gamma, color saturation adjust.
- Special effects included.
- Embedded 1.5V regulator for core power
- Target module size: 8 mm x 8 mm

2. Key Performance

Parameter		Value
Array Size		1280x 720
Power Supply	Digital	1.5V / 1.8V
	Analog	3.0V ~ 3.6V
	I/O	1.7V ~ 2.5V
Pixel Size		3.0 μm x 3.0 μm
Image Area		3840 μm x 2160 μm
ADC Resolution		10 bits
Shutter		Electronic Rolling Shutter
Frame Rate	HD (1280x720)	30 fps
Color Filter Arrays		RGB Bayer pattern
Maximum Data Rate		36 Mp/s
Maximum Clock Rate		72 MHz
Power Consumption		TBD
		Standby: < TBD μA

3. General Description

The NT99142 is a high performance image sensor. It incorporates a 1280 (H) x 720 (V) image array, an on-chip PLL oscillator and an on-chip 10 bits ADC, and embedded image signal processor. All the required image signal processing functions, including sharpness, noise reduction, defect correction, gamma, and color saturation adjust are supported. User can easily control through two-wire serial interface bus.

The NT99142 has a traditional parallel output port . It is suitable for Car Video Record, Wifi Camera, IP Camera and PC cameras applications.

4. Block Diagram

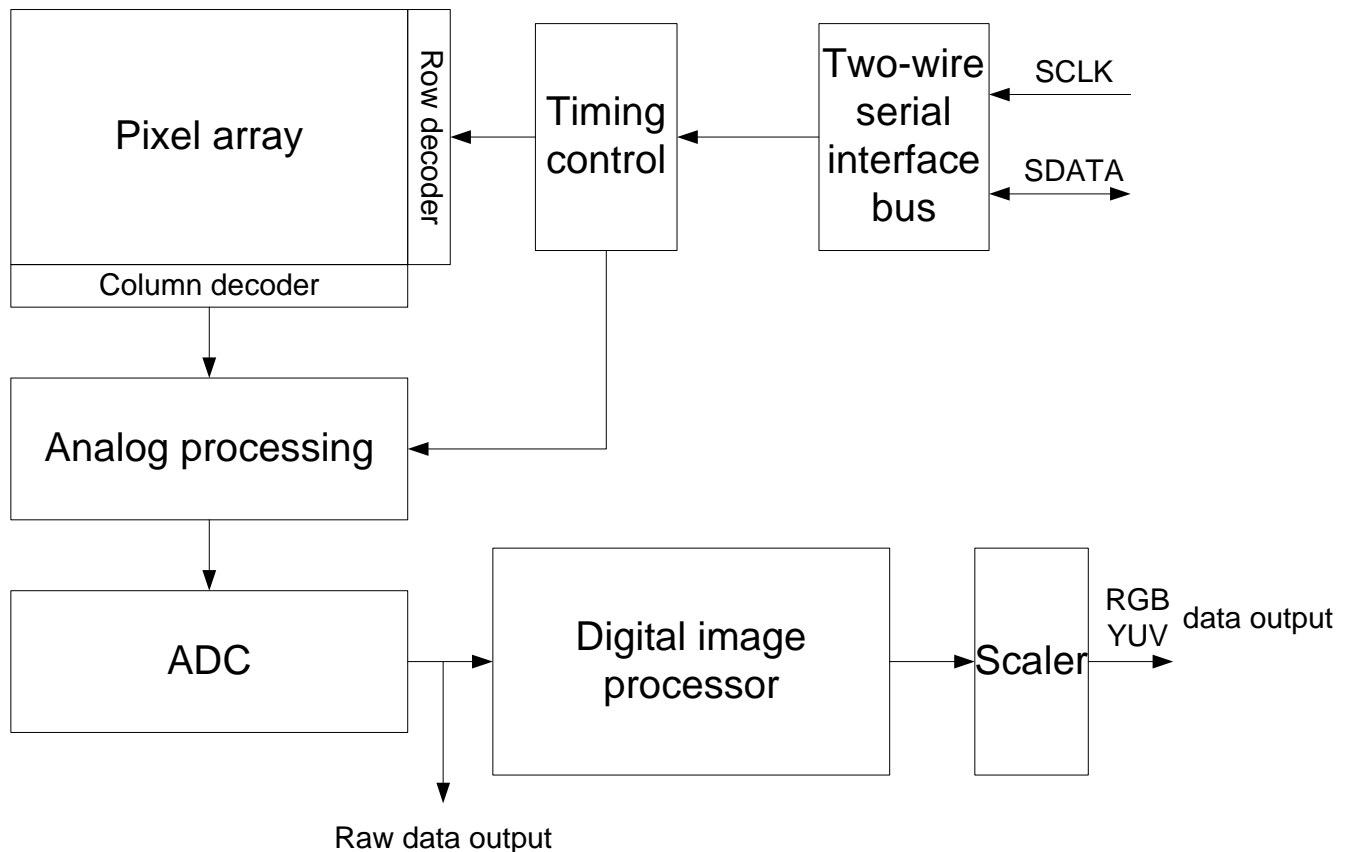


Fig. 1 Block Diagram

5. Pin Configuration

Top View

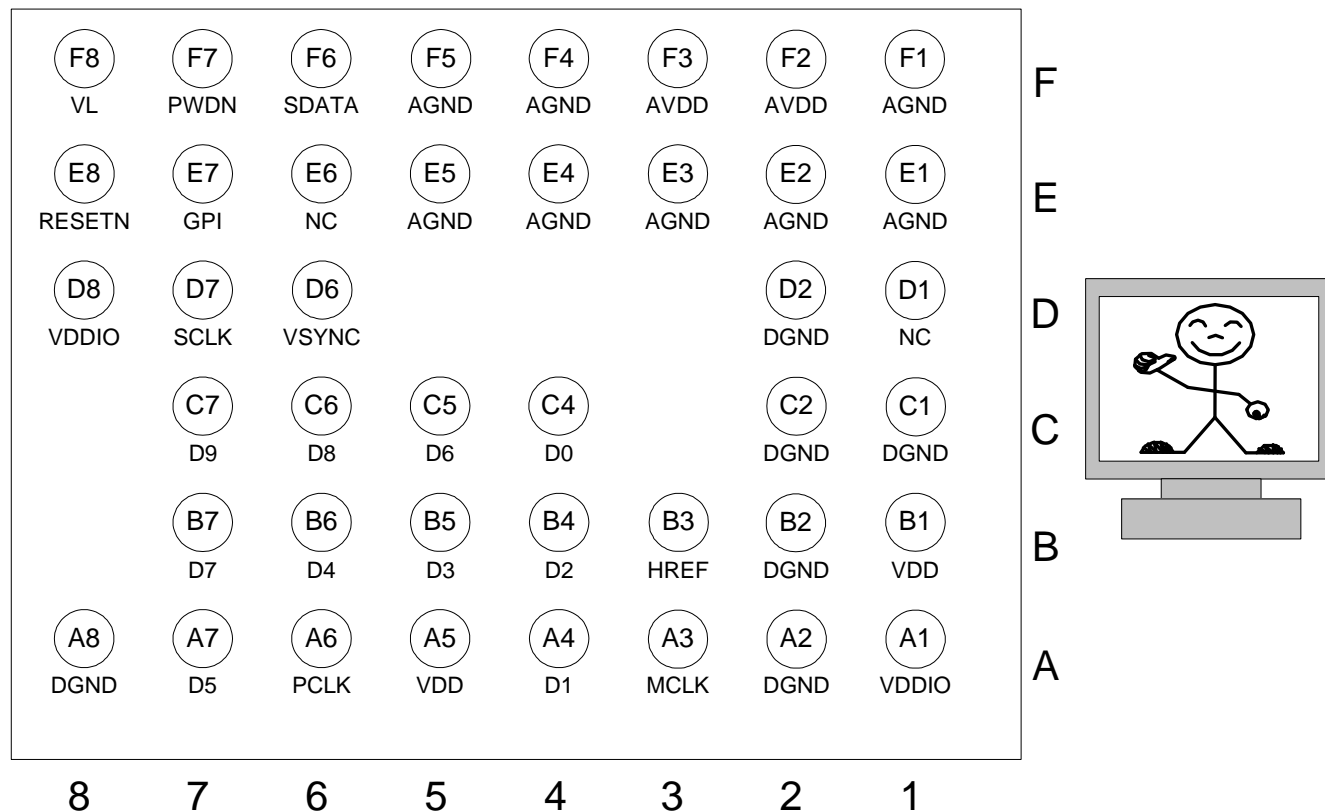


Fig. 2 Pin Configuration

6. Pin Descriptions

I = input port

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking

Pin No.	Name	Type	Descriptions
A1	VDDIO	Power	Digital power for I/O
A2	DGND	Ground	Digital ground
A3	MCLK	I	System clock input
A4	D1	O	Data output 1
A5	VDD	Power	Digital core power
A6	PCLK	O	Pixel clock output
A7	D5	O	Data output 5
A8	DGND	Ground	Digital ground

B1	VDD	Power	Digital core power
B2	DGND	Ground	Digital ground
B3	HREF	O	Horizontal reference
B4	D2	O	Data output 2
B5	D3	O	Data output 3
B6	D4	O	Data output 4
B7	D7	O	Data output 7
C1	DGND	Ground	Digital ground
C2	DGND	Ground	Digital ground
C4	D0	O	Data output 0
C5	D6	O	Data output 6
C6	D8	O	Data output 8
C7	D9	O	Data output 9
D1	NC	-	NC
D2	DGND	Ground	Digital ground
D6	VSNC	O	Vertical synchronization
D7	SCLK	I	Two-wire serial interface bus clock input
D8	VDDIO	Power	Digital power for I/O
E1	AGND	Ground	Analog ground
E2	AGND	Ground	Analog ground
E3	AGND	Ground	Analog ground
E4	AGND	Ground	Analog ground
E5	AGND	Ground	Analog ground
E6	NC	-	NC
E7	GPI	I	Only for multi-sensor function. Do not use, this pin must be connect to DGND.
E8	RESETN	I	Power on reset, active low 0: reset 1: normal
F1	AGND	Ground	Analog ground
F2	AVDD	Power	Analog power
F3	AVDD	Power	Analog power
F4	AGND	Ground	Analog ground
F5	AGND	Ground	Analog ground
F6	SDATA	I/O	Two-wire serial interface bus data I/O
F7	PWDN	I	Power down mode select, active high 0: normal mode 1: power down mode
F8	VL	-	Connect 0.1uF capacitor to AGND

D[9:0] is 10-bit Raw output(D9: MSB, D0: LSB)

7. Package Outline

	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	4862	4837	4887
Package Body Dimension Y	B	3822	3797	3847
Package Height	C	760	700	820
Ball Height	C1	130	100	160
Package Body Thickness	C2	630	585	675
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	250	220	280
Total Pin Count	N	42(2NC)		
Pin Count X axis	N1	8		
Pin Count Y axis	N2	6		
Pins Pitch X axis	J1	530		
Pins Pitch Y axis	J2	550		
Edge to Pin Center Distance along X	S1	576	546	606
Edge to Pin Center Distance along Y	S2	536	506	566

Mechanical Diagram

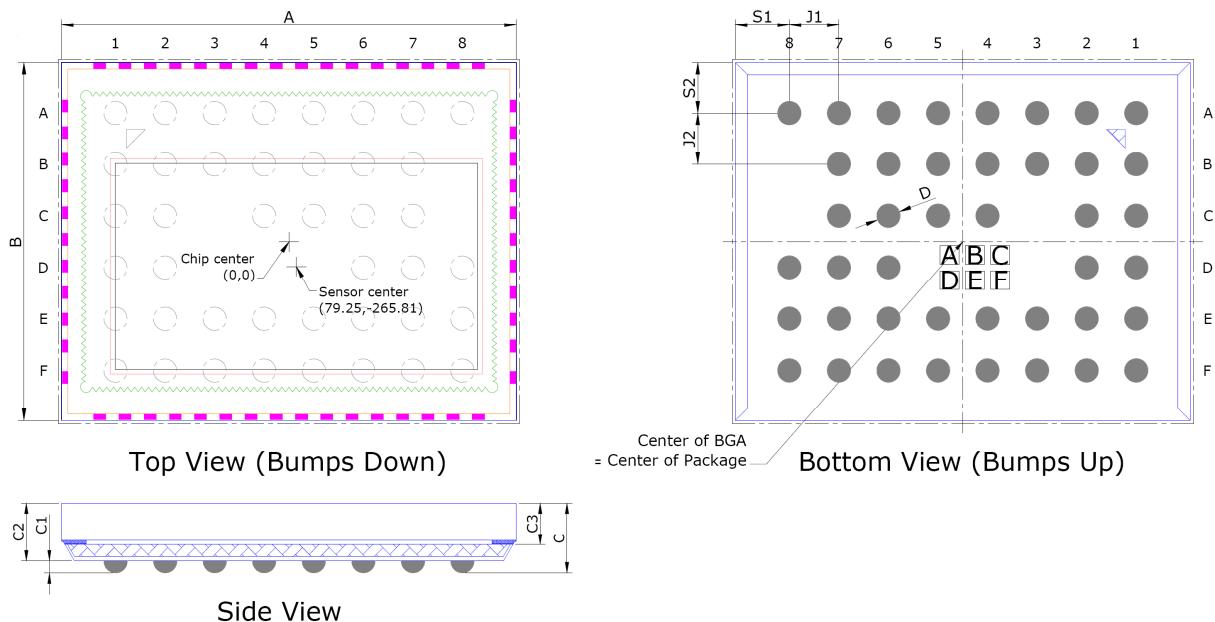


Fig. 3 Package Outline

8. Reference Circuit

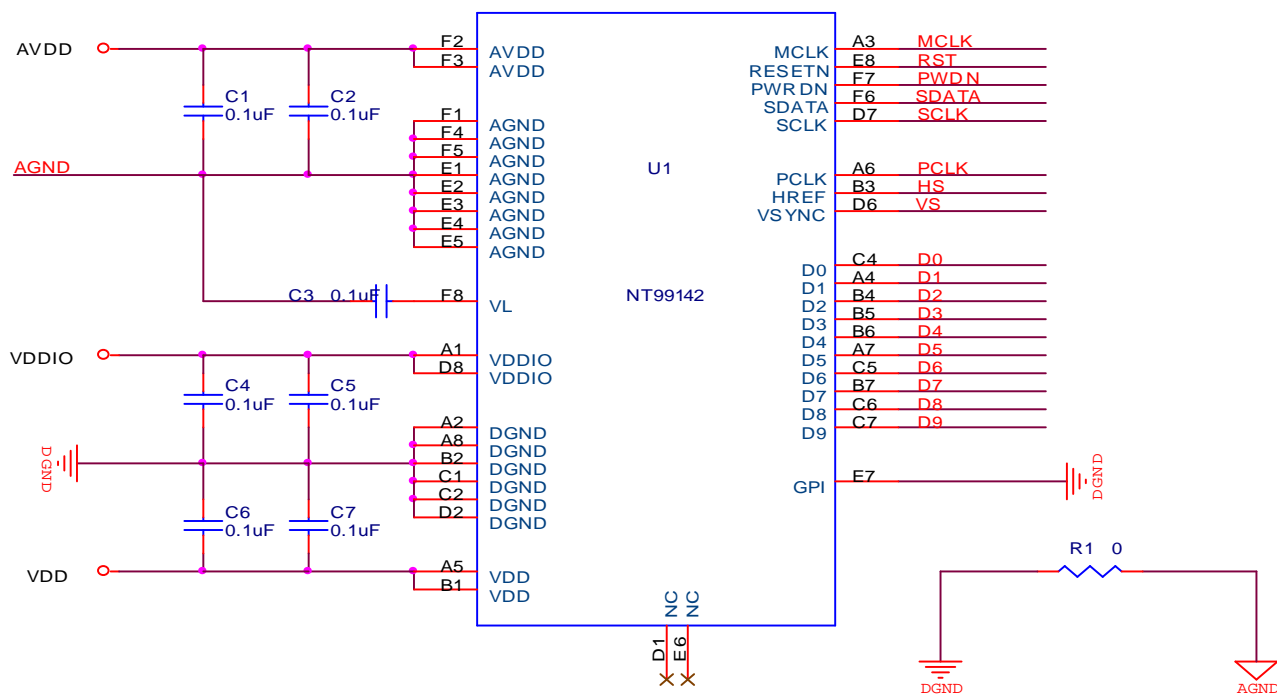


Fig. 4 Reference Circuit

- Note1 VDD is 1.5V of sensor digital core power.
- Note2 VDDIO is 1.7V~2.5V of sensor I/O power.
- Note3 AVDD is 3.0V~3.6V of sensor analog power.

9. Chief Ray Angle

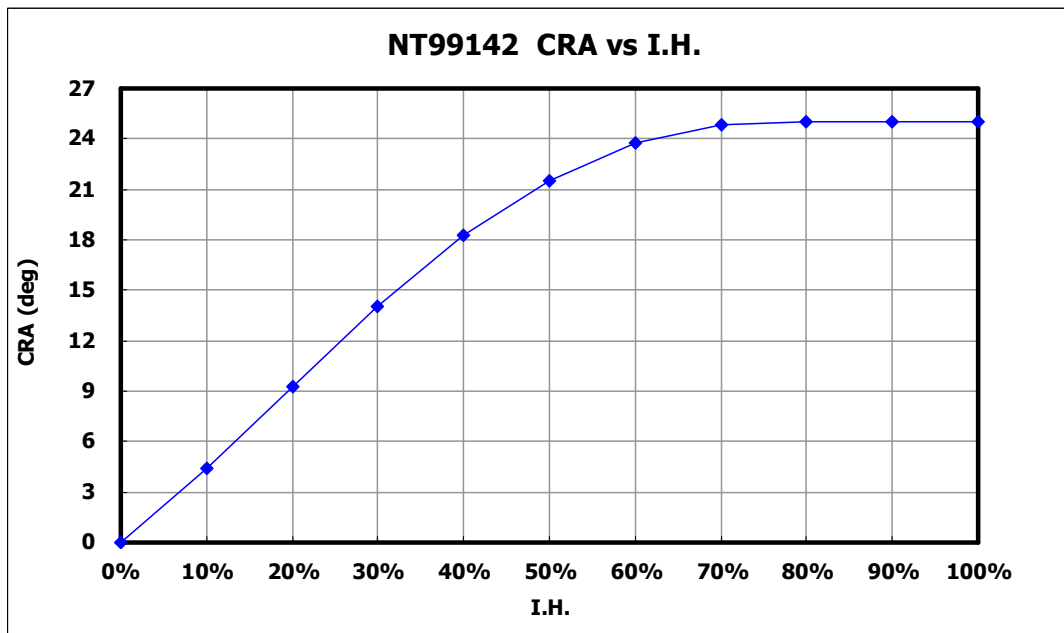


Fig. 5 Chief Ray Angle

10. SMT Reflow Profile

	A	B		C	D		E		F
	Ramp up	Pre-heat		Ramp up	Melt point		Peak point		Ramp down
		Temp.	Time		Temp.	Time	Temp.	Time	
New Reflow Profile	Max 3°C/sec	150 ~ 200°C	60~70 sec	Max 3°C/sec	217°C	60 ~70 sec	235 ~ 240°C	20~25 sec	Max 6°C/sec

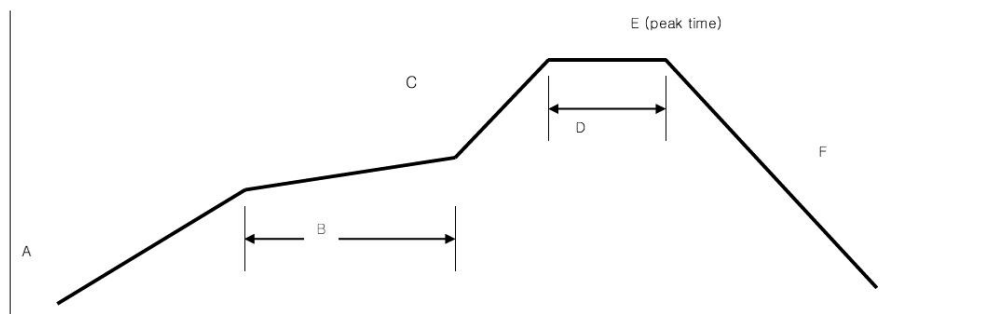


Fig. 6 SMT Reflow Profile